WHAT IS CLAIMED IS:

1. An addition circuit for digital data with:

   a digital adder for the addition of digital input data values which are present at data inputs of the digital adder to form a summation output data value, which is output at an output of the digital adder, the data inputs having a predetermined data bit width *n*, and

   a saturation circuit for limiting the summation output data value present at a data input of the saturation circuit within a data value range which is determined by an upper threshold data value and a lower threshold data value, the *n–m* least significant data bits of the summation output data value being present directly with the clock signal at the data input of the saturation circuit and the *m* most significant data bits of the summation output data value being switched through only with the inverted clock signal at the data input of the saturation circuit a clock-state-controlled latch register.

2. The addition circuit as claimed in claim 1, wherein input registers are provided for buffer-storing the digital input data values.

3. The addition circuit as claimed in claim 1, wherein an output register is provided for buffer-storing the summation output data value limited by the saturation circuit.

4. The addition circuit as claimed in claim 3, wherein the input registers and the output register are connected to a clock line for applying a clock signal.

5. The addition circuit as claimed in claim 1, wherein the clock-state-controlled latch register has a control input, which is connected to the clock signal line via an inverter circuit.

6. The addition circuit as claimed in claim 1, wherein the two threshold data values are settable.

7. The addition circuit as claimed in claim 1, wherein the saturation circuit has a first comparator for comparing the present summation output data value with the upper

threshold data value and a second comparator for comparing the present summation output data value with the lower threshold data value.

8. An addition circuit comprising:

a digital adder for the addition of digital input data values present at first and second data inputs thereof to form a summation output data value available at an adder output thereof, said summation output data value having a set of most significant bits and a set of least significant bits;

a clock-state-controlled latch register in communication with said adder output for receiving said set of most significant bits, said latch register having a latch output at which said set of most significant bits is made available in response to an inverted clock signal provided to a clock input of said latch register;

a saturation circuit having a saturation circuit output on which is made available a limited sum obtained by limiting said summation output data value to be within a data range defined by an upper threshold and a lower threshold, said saturation circuit being in communication with said latch register for receiving said set of most significant bits from said latch register in response to an inverted clock signal being provided to said latch register, and

being in communication with said output of said adder for receiving said set of least significant bits in response to a clock signal being provided to said adder.

9. The addition circuit of claim 8, further comprising first and second input registers for buffering said digital input data values, said first and second input registers being in communication with said first and second data inputs of said adder.

10. The addition circuit of claim 8, further comprising an output register in communication with said saturation circuit output for buffering said saturation circuit output.

11. The addition circuit of claim 10, further comprising a clock line connected to said first and second input registers and to said output register.

12. The addition circuit of claim 8, further comprising an inverter circuit having an inverter input for receiving a clock signal and an inverter output in communication with said latch register for making available to said latch register an inverted clock signal.

13. The addition circuit of claim 8, wherein said saturation circuit further comprises an interface for enabling said upper threshold and said lower threshold to be settable.

14. The addition circuit of claim 8, wherein said saturation circuit comprises a comparator having a first input on which is provided a threshold selected from said upper threshold and said lower threshold and a second input on which is provided said summation output data value, said comparator being configured to compare said threshold with said summation output data value.